



FIG. 1
PRIOR ART

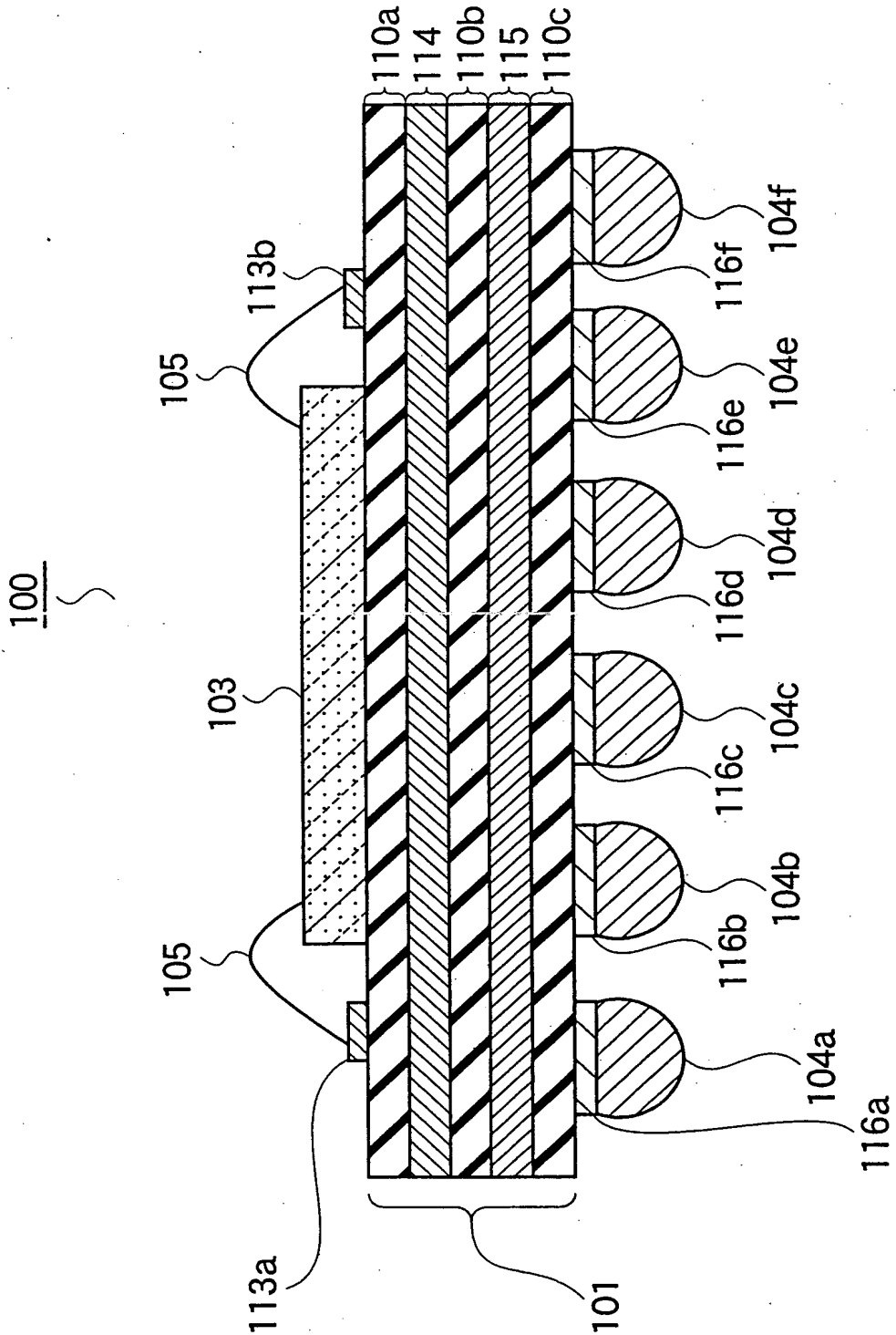


FIG. 2
PRIOR ART

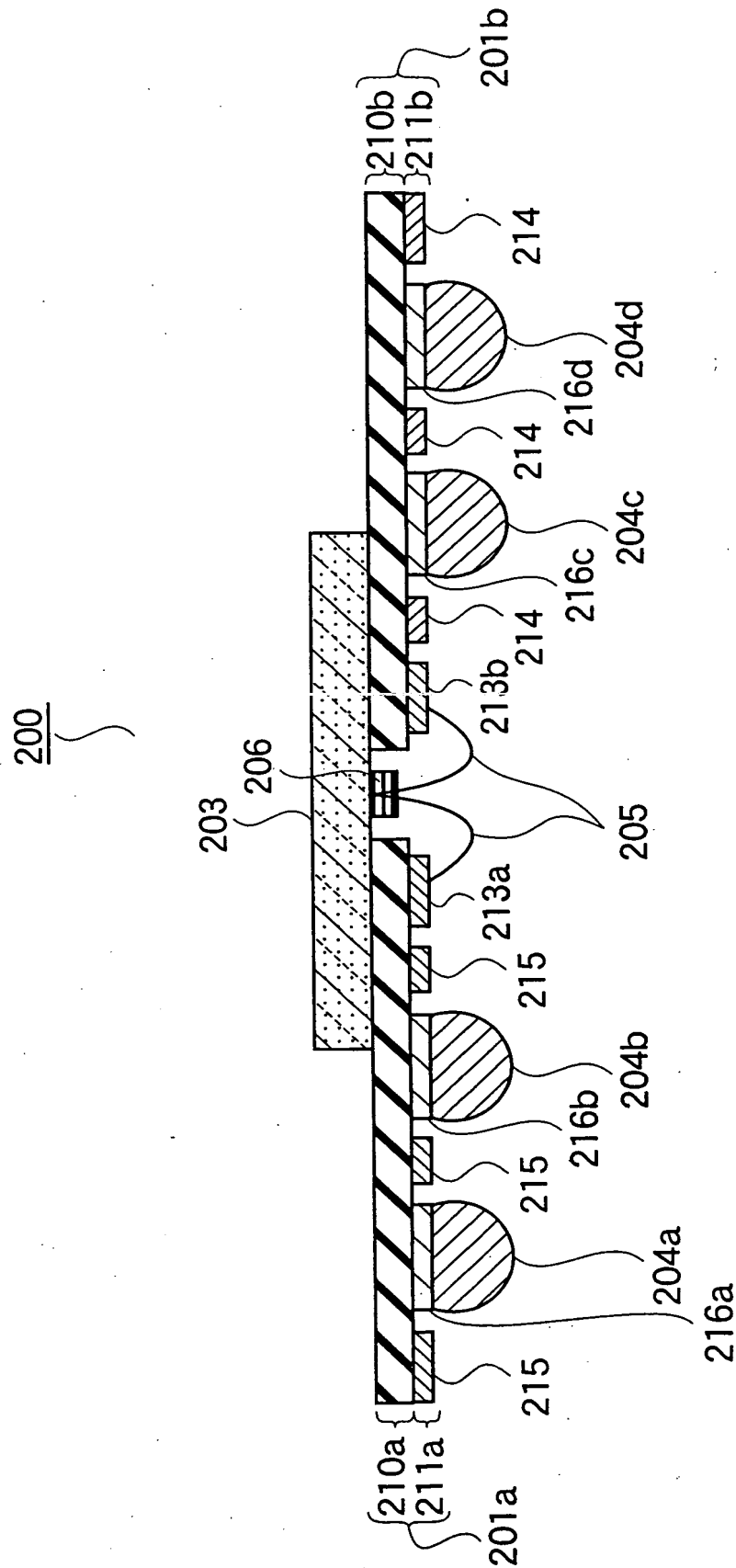
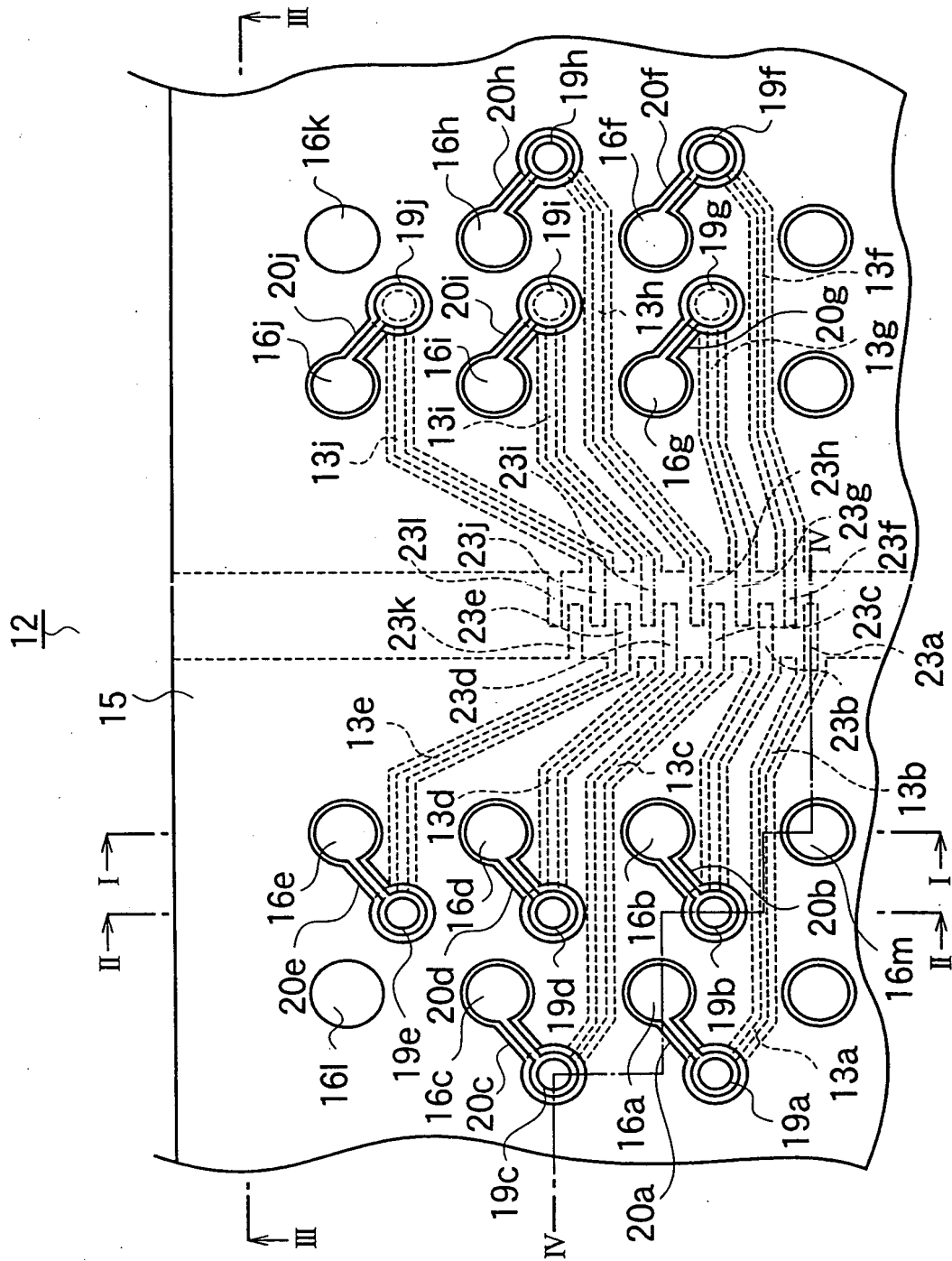


FIG. 4



5/13

FIG. 5

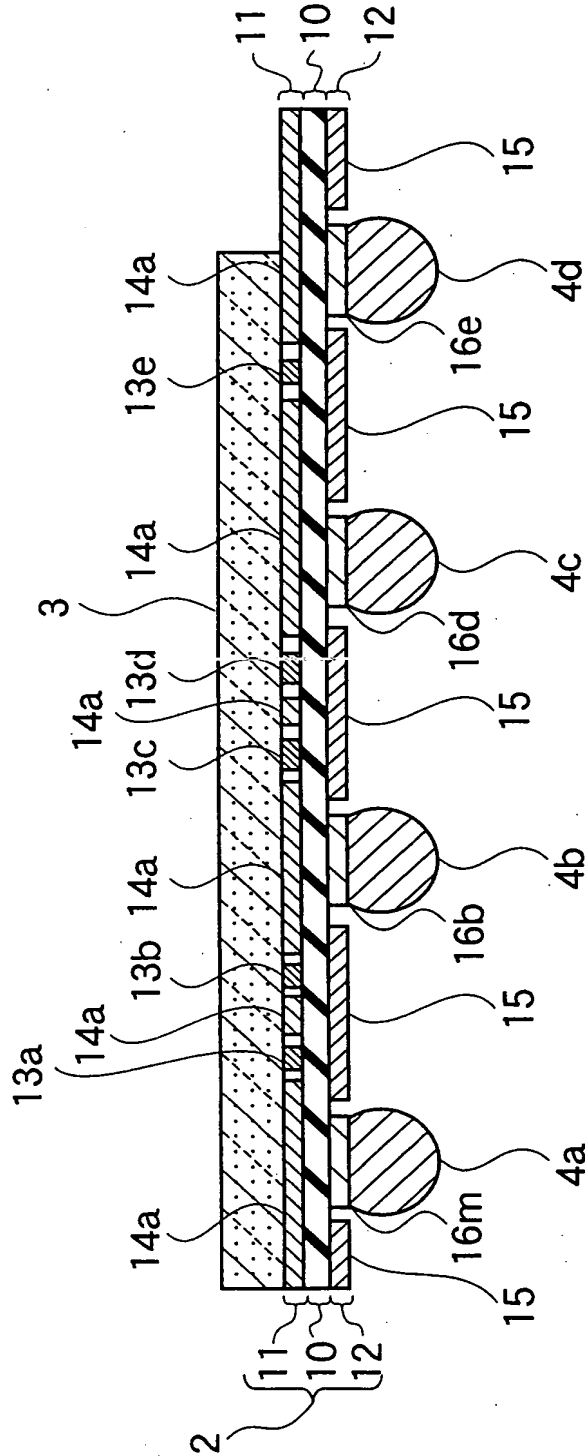
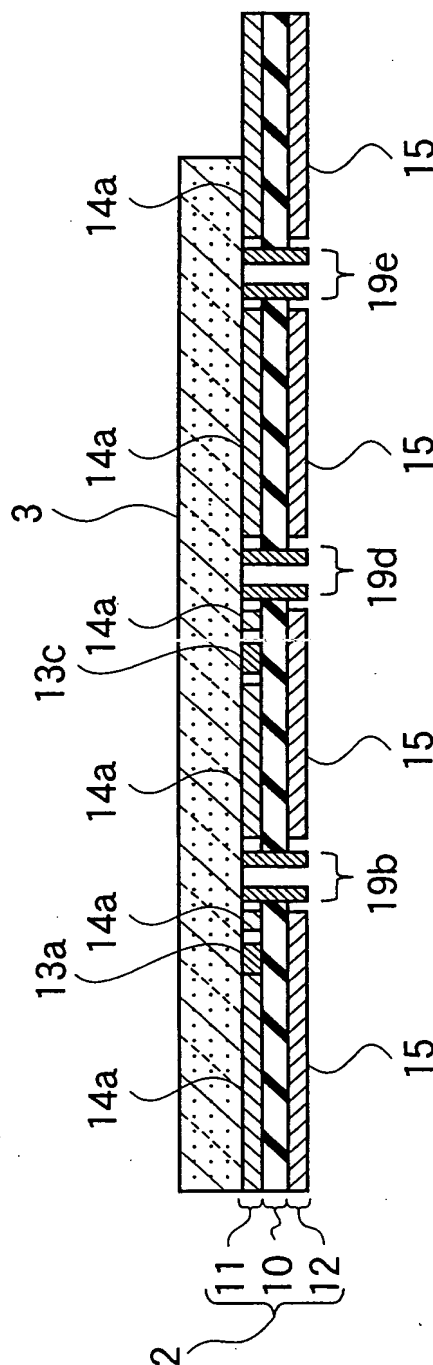
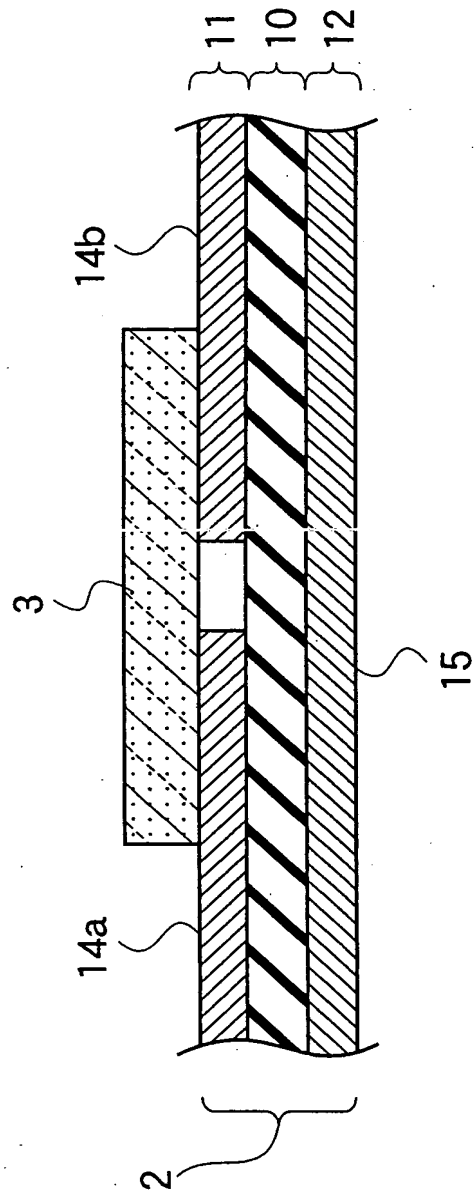


FIG. 6



7/13

FIG. 7



8/13

FIG. 8A

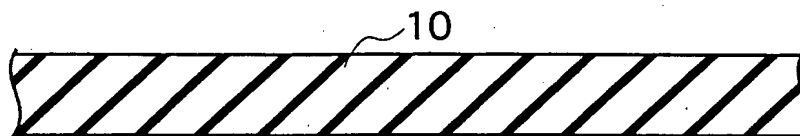


FIG. 8B



FIG. 8C

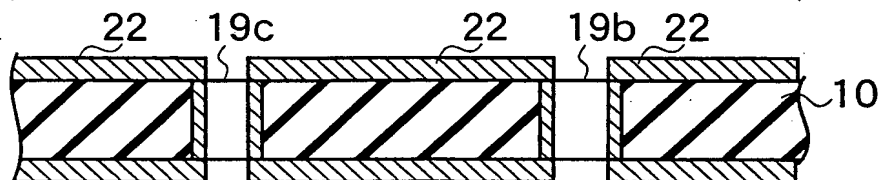


FIG. 8D

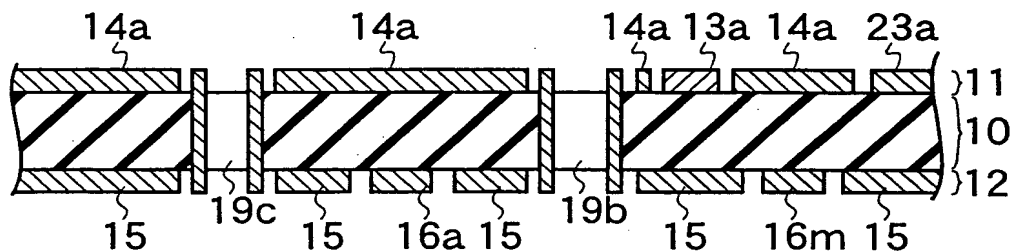


FIG. 8E

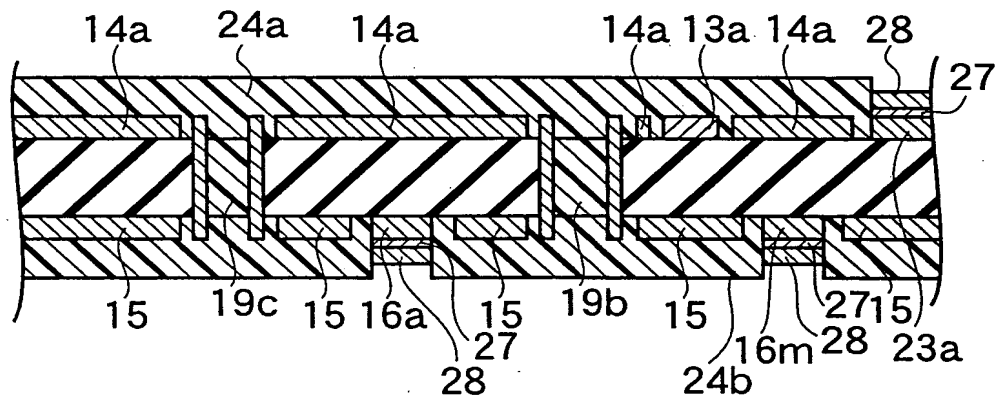
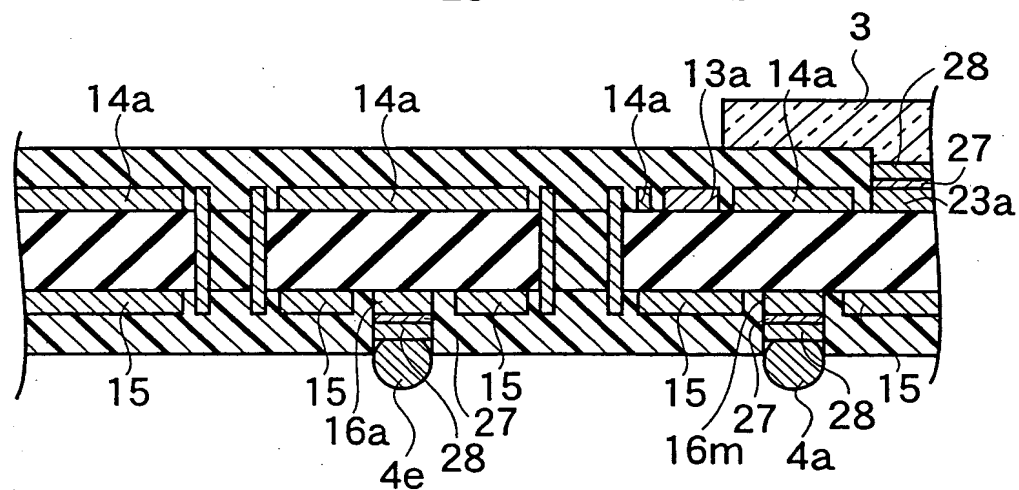


FIG. 8F



9/13

FIG. 9

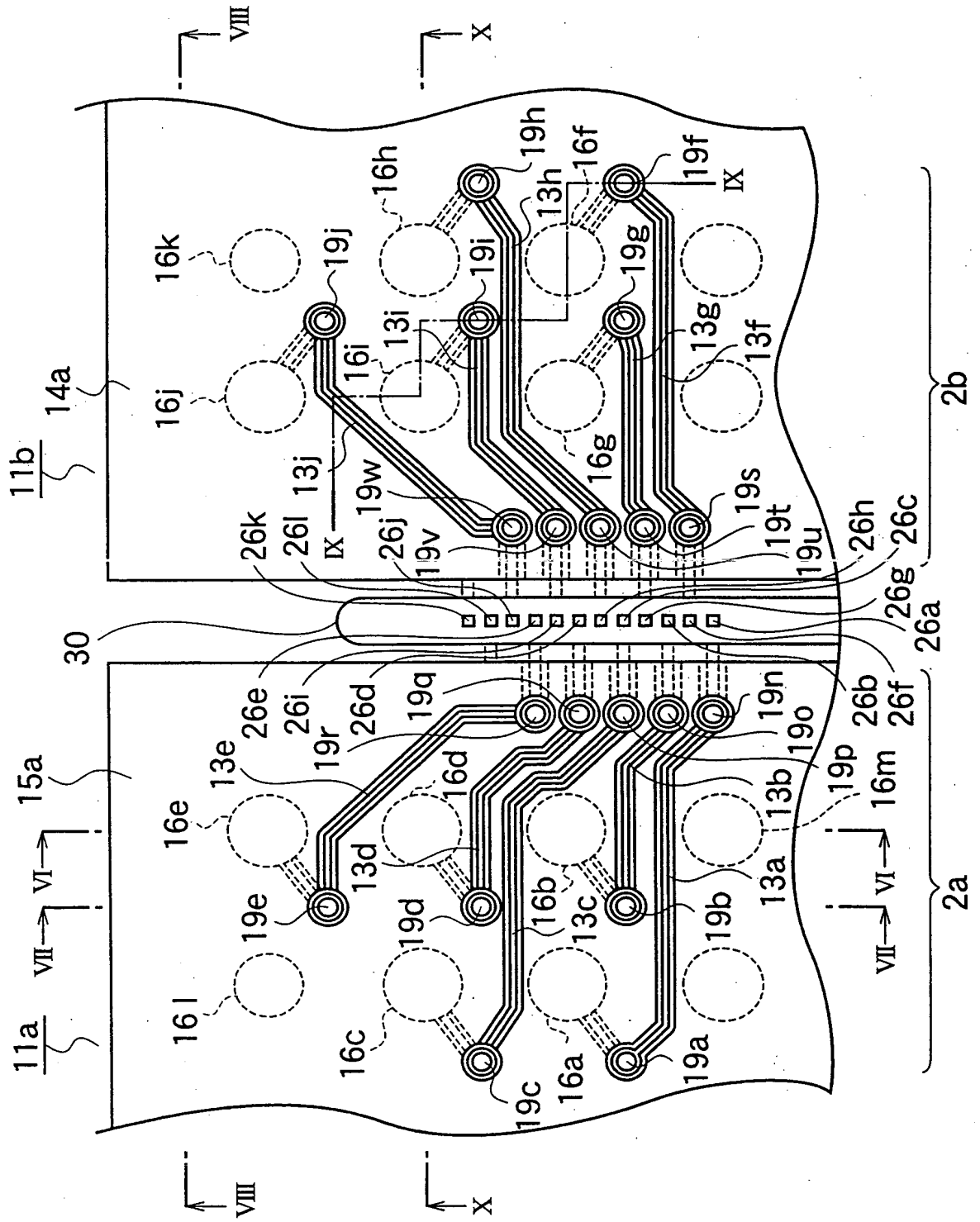
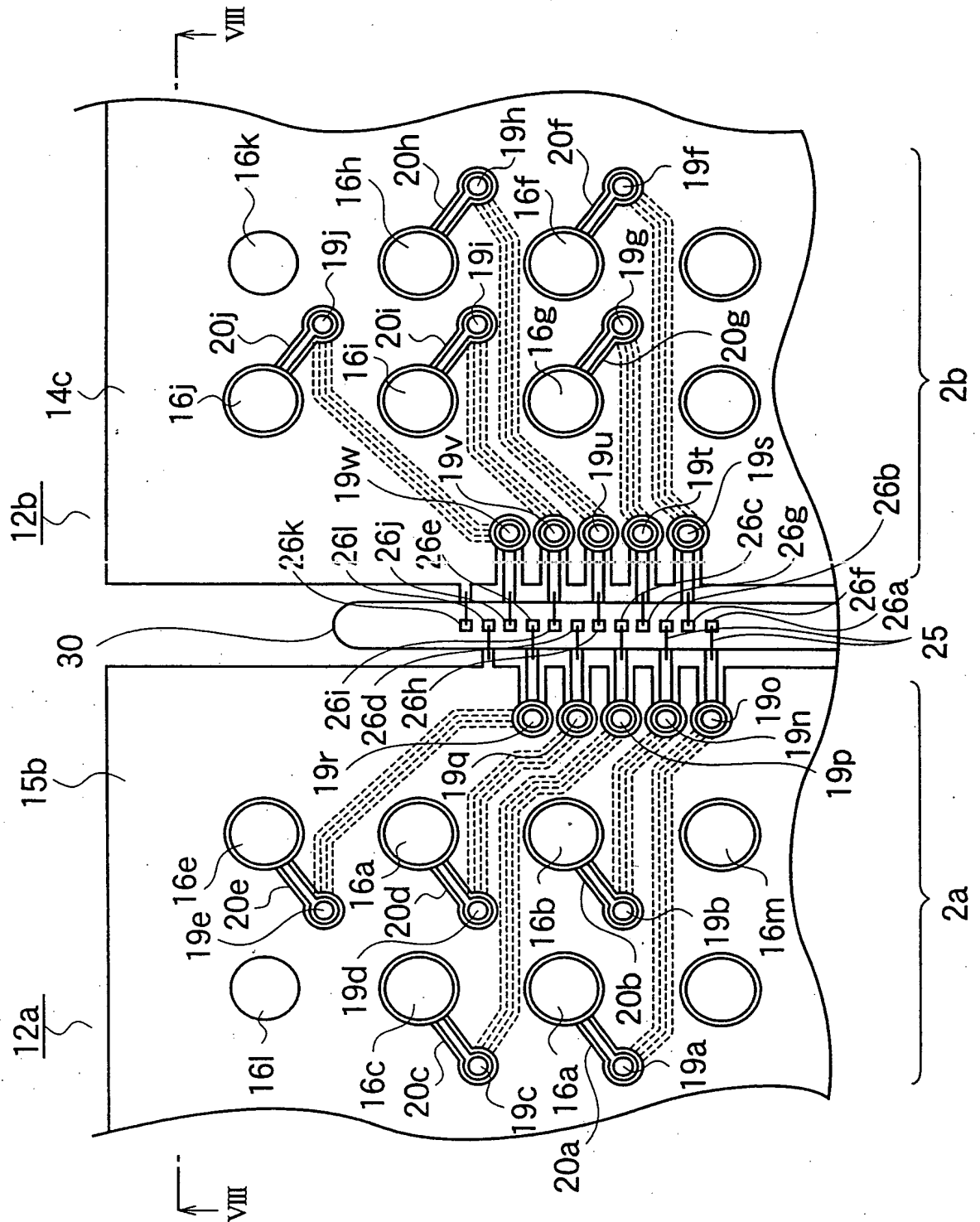


FIG. 10



11/13

FIG. 11

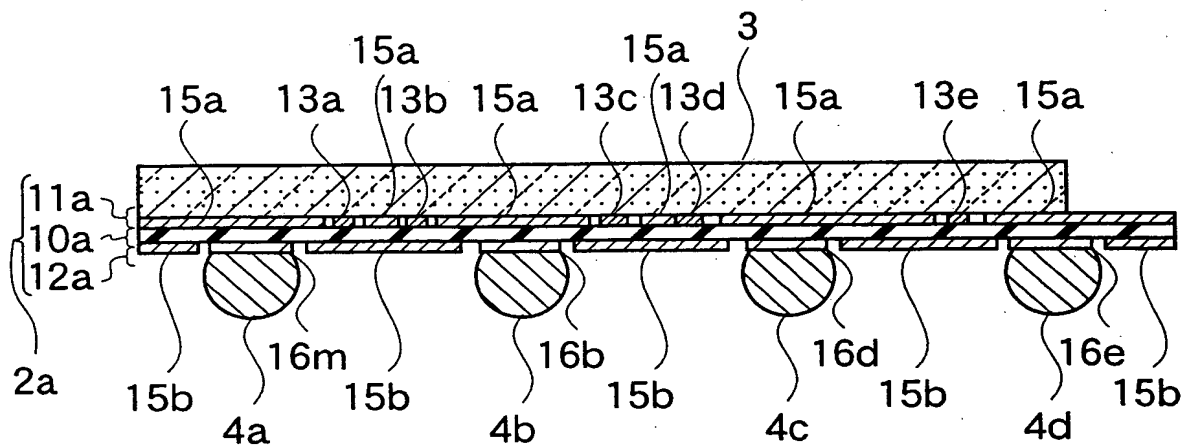


FIG. 12

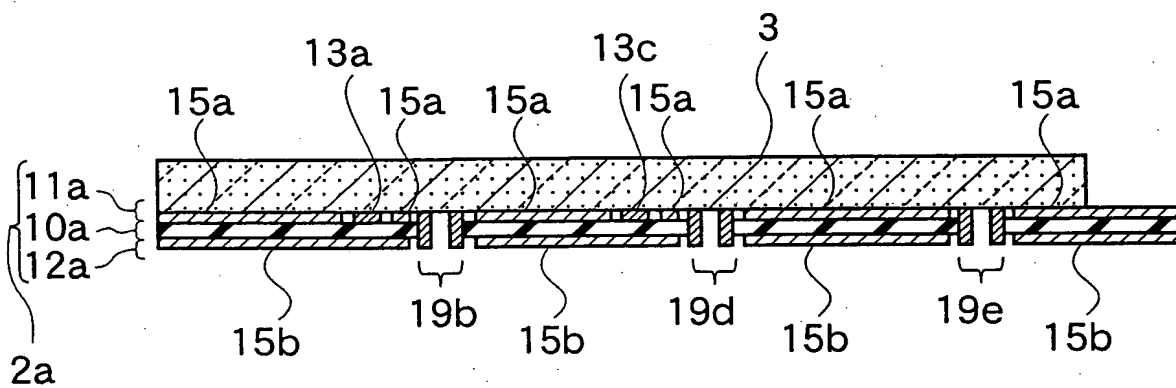
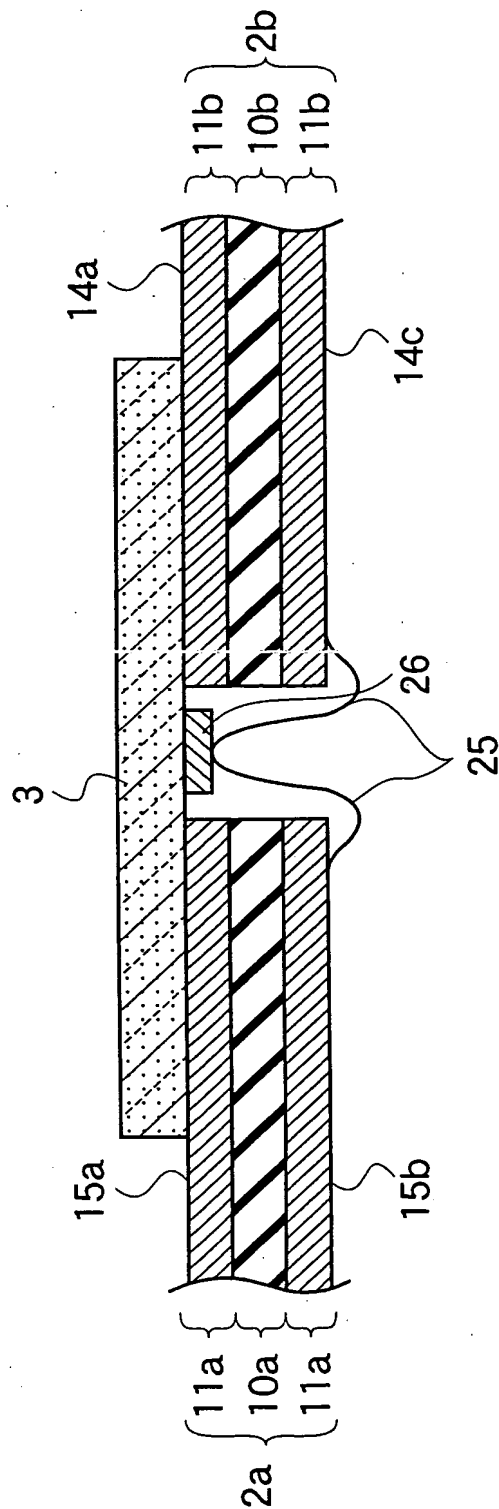


FIG. 13



A cross-sectional view of a second layer 10b, which is a hatched rectangular layer positioned below the first layer 10a.

A cross-sectional view of a portion of the device, showing a repeating pattern of layers. The layers are labeled 19i, 10b, and 19f. Layer 19i is a hatched layer, layer 10b is a solid white layer, and layer 19f is a hatched layer. The layers are stacked vertically, with 19i at the bottom, 10b in the middle, and 19f at the top. The pattern repeats across the width of the device.

A cross-sectional view of a segmented strip assembly 10b. It consists of three rectangular segments, each labeled 22, which are joined by two vertical interfaces labeled 19i and 19f. The segments 22 are filled with diagonal hatching. The entire assembly is bounded by a horizontal line at the top and bottom, with the rightmost end labeled 10b.

A cross-sectional view of a semiconductor device. The device consists of a central channel region (10b) flanked by side regions (11b and 12b). The channel region (10b) is formed in a substrate (13h) and is covered by a layer (14a). The side regions (11b and 12b) are also covered by a layer (14a). The device includes various contacts and interconnects, labeled 14a, 13j, 14a, 19i, 13h, 14a, 19f, and 14a. The layers 11b, 10b, and 12b are indicated by brackets on the right side of the diagram.

[illegible]